WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor chip;

a layer with low electrical resistance of a first conductivity type or a second conductivity type in the bottom portion of the semiconductor chip;

a breakdown-voltage sustaining layer above the layer with low electrical resistance, the breakdown-voltage sustaining layer comprising at least one or more semiconductor regions of the first conductivity type;

a well region of the second conductivity type in the surface portion of the breakdown-voltage sustaining layer;

a source region of the first conductivity type in the surface portion of the well region;

surface regions of the first conductivity type, the surface regions being the extended portions of the breakdown-voltage sustaining layer extended to the surface of the semiconductor chip and surrounded by the well region;

a gate electrode above the extended portion of the well region extended between the surface region and the source region with a gate insulation film interposed therebetween;

a source electrode in contact commonly with the source region and the well region;

a drain electrode on the back surface of the layer with low electrical resistance; and

wherein the ratio between the total surface area of the surface regions and the surface area of the well region including the source region being from 0.01 to 0.2.

2. A semiconductor device comprising:

a semiconductor chip;

a layer with low electrical resistance of a first conductivity type or a second conductivity type in the bottom portion of the semiconductor chip;

a breakdown-voltage sustaining layer above the layer with low electrical resistance, the breakdown-voltage sustaining layer comprising at least one or more semiconductor regions of the first conductivity type;

a well region of the second conductivity type in the surface portion of the breakdown-voltage sustaining layer;

a source region of the first conductivity type in the surface portion of the well region;

surface regions of the first conductivity type, the surface regions being the extended portions of the breakdown-voltage sustaining layer extended to the surface of the semiconductor chip and surrounded by the well region;

a gate electrode above the extended portion of the well region extended between the surface region and the source region with a gate insulation film interposed therebetween;

a source electrode in contact commonly with the source region and the well region;

a drain electrode on the back surface of the layer with low electrical resistance; and

wherein the shape of the surface regions in the surface of the semiconductor chip is a long stripe.

3. The semiconductor device according to Claim 2, wherein the stripe of the surface region is from 0.1 to 2 μm in width in the main portion thereof.

4. The semiconductor device according to Claim 2, wherein the ratio between the total surface area of the surface regions and the surface area of the well region including the source region is from 0.01 to 0.2.

5. The semiconductor device according to Claim 2, wherein the stripe of the surface region is 100 μm or longer.

6. The semiconductor device according to Claim 5, wherein the stripe of the surface region is 500 μm or longer.

7. The semiconductor device according to Claim 2, wherein the stripe of the surface region includes a plurality of convex portion extending from the stripe in the different direction different from the extending direction of the stripe of the surface region.

8. The semiconductor device according to Claim 7, wherein the stripe of the surface region includes one or less convex portion for every 50 μm thereof.

9. The semiconductor device according to Claim 7, wherein the stripe of the surface region includes one or less convex portion for every 250 μm thereof.

10. The semiconductor device according to Claim 7, wherein the convex portion extends for 2 μm or less from the stripe of the surface region.

11. A semiconductor device comprising:

a semiconductor chip;

a layer with low electrical resistance of a first conductivity type or a second conductivity type in the bottom portion of the semiconductor chip;

a breakdown-voltage sustaining layer above the layer with low electrical resistance, the breakdown-voltage sustaining layer comprising at least one or more semiconductor regions of the first conductivity type;

a well region of the second conductivity type in the surface portion of the breakdown-voltage sustaining layer;

a source region of the first conductivity type in the surface portion of the well region;

surface regions of the first conductivity type, the surface regions being the extended portions of the breakdown-voltage sustaining layer extended to the surface of the semiconductor chip and surrounded by the well region;

a gate electrode above the extended portion of the well region extended between the surface region and the source region with a gate insulation film interposed therebetween;

a source electrode in contact commonly with the source region and the well region;

a drain electrode on the back surface of the layer with low electrical resistance; and

wherein the gate electrode comprises a plurality of stripes, each surrounded by the well region in a plane parallel to the surface of the semiconductor chip.

12. The semiconductor device according to Claim 11, wherein each of the stripes of the gate electrode covers one or more surface regions.

13. The semiconductor device according to Claim 11, wherein each of the stripes of the gate electrode is from 4 to 8 μm in width in the main portion thereof.

14. The semiconductor device according to Claim 13, wherein each of the stripes of the gate electrode is from 5 to 7 μm in width in the main portion thereof.

15. The semiconductor device according to Claim 11, wherein the stripes of the gate electrode are 100 μm or longer in length.

16. The semiconductor device according to Claim 15, wherein the stripes of the gate electrode are 500 μm or longer in length.

17. The semiconductor device according to Claim 11, wherein the gate electrode comprises narrow bridges connecting the stripes thereof.

18. The semiconductor device according to Claim 17, wherein the bridges are 4 μm or less in width.

19. The semiconductor device according to Claim 17, wherein the well region is extended below the main portions of the bridges of the gate electrode.

20. The semiconductor device according to Claim 17, wherein one or less bridge is formed for every 50 μm of the stripe of the gate electrode.

21. The semiconductor device according to Claim 20, wherein one or less bridge is formed for every 250 μm of the stripe of the gate electrode.

22. The semiconductor device according to Claim 1, wherein the breakdown-voltage sustaining layer comprises semiconductor regions of the first conductivity type and semiconductor regions of the second conductivity type arranged alternately.

23. The semiconductor device according to Claim 2, wherein the breakdown-voltage sustaining layer comprises semiconductor regions of the first conductivity type and semiconductor regions of the second conductivity type arranged alternately.

24. The semiconductor device according to Claim 11, wherein the breakdown-voltage sustaining layer comprises semiconductor regions of the first conductivity type and semiconductor regions of the second conductivity type arranged alternately.

25. The semiconductor device according to Claim 1, wherein the resistivity in the portions of the surface regions shallower than the well region is lower than the resistivity in the portion of the breakdown-voltage sustaining layer deeper than the well region.

26. The semiconductor device according to Claim 2, wherein the resistivity in the portions of the surface regions shallower than the well region is lower than the

resistivity in the portion of the breakdown-voltage sustaining layer deeper than the well region.

27. The semiconductor device according to Claim 11, wherein the resistivity in the portions of the surface regions shallower than the well region is lower than the resistivity in the portion of the breakdown-voltage sustaining layer deeper than the well region.

28. The semiconductor device according to Claim 25, wherein the doping amount of the impurity of the first conductivity type in the surface regions is from 2 x 10^{12} cm^{-2} to 5 x 10^{12} cm^{-2}.

29. The semiconductor device according to Claim 26, wherein the doping amount of the impurity of the first conductivity type in the surface regions is from 2 x 10^{12} cm^{-2} to 5 x 10^{12} cm^{-2}.

30. The semiconductor device according to Claim 27, wherein the doping amount of the impurity of the first conductivity type in the surface regions is from 2 x 10^{12} cm^{-2} to 5 x 10^{12} cm^{-2}.

31. The semiconductor device according to Claim 28, wherein the doping amount is from 2.5 x 10^{12} cm^{-2} to 4 x 10^{12} cm^{-2}.

32. The semiconductor device according to Claim 29, wherein the doping amount is from 2.5 x 10^{12} cm^{-2} to 4 x 10^{12} cm^{-2}.

33. The semiconductor device according to Claim 30, wherein the doping amount is from 2.5 x 10^{12} cm^{-2} to 4 x 10^{12} cm^{-2}.

34. A semiconductor device comprising:

a semiconductor chip;

a layer with low electrical resistance of a first conductivity type or a second conductivity type in the bottom portion of the semiconductor chip;

a breakdown-voltage sustaining layer above the layer with low electrical resistance, the breakdown-voltage sustaining layer comprising at least one or more semiconductor regions of the first conductivity type;

a well region of the second conductivity type in the surface portion of the breakdown-voltage sustaining layer; and

guard rings of the second conductivity type in the surface portion of the semiconductor chip, the guard rings surroundings the well region;

wherein the number of the guard rings is equal to or more than the number n calculated by the following equation;

$n = 1.0 \times Vbr/100$; and

wherein Vbr (V) is the breakdown voltage of the semiconductor device.

35. The semiconductor device according to Claim 34, wherein the number of the guard rings is equal to or more than the number n calculated by the following equation,

$n = 1.5 \times Vbr/100$.

36. The semiconductor device according to Claim 34, wherein the number of the guard rings is equal to or less than the number n calculated by the following equation,

$n = 6.0 \times Vbr/100$.

37. A semiconductor device comprising:

a semiconductor chip;

a layer with low electrical resistance of a first conductivity type or a second conductivity type in the bottom portion of the semiconductor chip;

a breakdown-voltage sustaining layer above the layer with low electrical resistance, the breakdown-voltage sustaining layer comprising at least one or more semiconductor regions of the first conductivity type;

a well region of the second conductivity type in the surface portion of the breakdown-voltage sustaining layer;

guard rings of the second conductivity type in the surface portion of the semiconductor chip, the guard rings surroundings the well region; and

wherein the spacing between the well region and the first guard ring nearest to the well region being 1 μm or less.

38. The semiconductor device according to Claim 34, wherein the spacing between the well region and the first guard ring nearest to the well region is 1 μm or less.

39. The semiconductor device according to Claim 37, wherein the spacing between the well region and the first guard ring is 0.5 μm or lessr.

40. The semiconductor device according to Claim 38, wherein the spacing between the well region and the first guard ring is 0.5 μm or less.

41. The semiconductor device according to Claim 39, wherein the first guard ring is in contact with the well region.

42. The semiconductor device according to Claim 40, wherein the first guard ring is in contact with the well region.

43. The semiconductor device according to Claim 37, wherein the spacing between the first guard ring and the second guard ring second nearest to the well region is 1.5 μm or less.

44. The semiconductor device according to Claim 38, wherein the spacing between the first guard ring and the second guard ring second nearest to the well region is 1.5 μm or less.

45. The semiconductor device according to Claim 43, wherein the spacing between the first guard ring and the second guard is 1 μm or less.

46. The semiconductor device according to Claim 44, wherein the spacing between the first guard ring and the second guard is 1 μm or lessr.

47. The semiconductor device according to Claim 45, wherein the spacing between the first guard ring and the second guard ring is 0.5 μm or less.

48. The semiconductor device according to Claim 46, wherein the spacing between the first guard ring and the second guard ring is 0.5 μm or less.

49. The semiconductor device according to Claim 43, wherein the spacing between the second guard ring and the third guard ring third nearest to the well region is 2.0 μm or less.

50. The semiconductor device according to Claim 44, wherein the spacing between the second guard ring and the third guard ring third nearest to the well region is 2.0 μm or less.

51. The semiconductor device according to Claim 49, wherein the spacing between the second guard ring and the third guard ring is 1.0 μm or less.

52. The semiconductor device according to Claim 50, wherein the spacing between the second guard ring and the third guard ring is 1.0 μm or less.

53. The semiconductor device according to Claim 49, wherein the spacing between the third guard ring and the fourth guard ring fourth nearest to the well region is 2.5 μm or less.

54. The semiconductor device according to Claim 50, wherein the spacing between the third guard ring and the fourth guard ring fourth nearest to the well region is 2.5 μm or less.

55. The semiconductor device according to Claim 53, wherein the spacing between the third guard ring and the fourth guard ring is 2.0 μm or less.

56. The semiconductor device according to Claim 54, wherein the spacing between the third guard ring and the fourth guard ring is 2.0 μm or less.

57. A semiconductor device comprising:

a semiconductor chip;

a layer with low electrical resistance of a first conductivity type or a second conductivity type in the bottom portion of the semiconductor chip;

a breakdown-voltage sustaining layer above the layer with low electrical resistance, the breakdown-voltage sustaining layer comprising at least one or more semiconductor regions of the first conductivity type;

a well region of the second conductivity type in the surface portion of the breakdown-voltage sustaining layer;

guard rings of the second conductivity type in the surface portion of the semiconductor chip, the guard rings surroundings the well region; and

wherein the spacing between the well region and the first guard ring nearest to the well region being $d_1/4$ or less, said d_1 being a shallower one of the junction depth of the well region and the junction depth of the guard rings.

58. The semiconductor device according to Claim 34, wherein the spacing between the well region and the first guard ring nearest to the well region is $d_1/4$ or less, where said d_1 is a shallower one of the junction depth of the well region and the junction depth of the guard rings.

59. The semiconductor device according to Claim 57, wherein the spacing between the well region and the first guard ring is $d_1/8$ or less.

60. The semiconductor device according to Claim 58, wherein the spacing between the well region and the first guard ring is $d_1/8$ or less.

61. The semiconductor device according to Claim 57, wherein the spacing between the first guard ring and the second guard ring second nearest to the well region is $d_2/4$ or less, where said d_2 is the junction depth of the guard rings.

62. The semiconductor device according to Claim 58, wherein the spacing between the first guard ring and the second guard ring second nearest to the well region is $d_2/4$ or less, where said d_2 is the junction depth of the guard rings.

63. The semiconductor device according to Claim 61, wherein the spacing between the first guard ring and the second guard ring is $d_2/8$ or less.

64. The semiconductor device according to Claim 62, wherein the spacing between the first guard ring and the second guard ring is $d_2/8$ or less.

65. The semiconductor device according to Claim 61, wherein the spacing between the second guard ring and the third guard ring third nearest to the well region is $d_2/4$ or less.

66. The semiconductor device according to Claim 62, wherein the spacing between the second guard ring and the third guard ring third nearest to the well region is $d_2/4$ or less.

67. The semiconductor device according to Claim 65, wherein the spacing between the second guard ring and the third guard ring is $d_2/8$ or less.

68. The semiconductor device according to Claim 66, wherein the spacing between the second guard ring and the third guard ring is $d_2/8$ or less.

69. The semiconductor device according to Claim 34, wherein the difference I_2-I_1 between the spacing I_2 between the first guard ring nearest to the well region and the second guard ring second nearest to the well region and the spacing I_1 between the well region and the first guard ring is 1 μm or less.

70. The semiconductor device according to Claim 37, wherein the difference I_2-I_1 between the spacing I_2 between the first guard ring nearest to the well region and the second guard ring second nearest to the well region and the spacing I_1 between the well region and the first guard ring is 1 μm or less.

71. The semiconductor device according to Claim 57, wherein the difference I_2-I_1 between the spacing I_2 between the first guard ring nearest to the well region and the second guard ring second nearest to the well region and the spacing I_1 between the well region and the first guard ring is 1 μm or less.

72. The semiconductor device according to Claim 69, wherein the difference I_2 -I_1 is from 0.2 to 0.8 μm.

73. The semiconductor device according to Claim 70, wherein the difference I_2-I_1 is from 0.2 to 0.8 μm.

74. The semiconductor device according to Claim 71, wherein the difference I_2-I_1 is from 0.2 to 0.8 μm.

75. The semiconductor device according to Claim 69, wherein the difference I_3-I_2 between the spacing I_3 between the second guard ring and the third guard ring third nearest to the well region and the spacing I_2 between the first guard ring and the second guard ring is 1 μm or less.

76. The semiconductor device according to Claim 70, wherein the difference I_3-I_2 between the spacing I_3 between the second guard ring and the third guard ring third nearest to the well region and the spacing I_2 between the first guard ring and the second guard ring is 1 μm or less.

77. The semiconductor device according to Claim 71, wherein the difference I_3-I_2 between the spacing I_3 between the second guard ring and the third guard ring third nearest to the well region and the spacing I_2 between the first guard ring and the second guard ring is 1 μm or less.

78. The semiconductor device according to Claim 75, wherein the difference I_3-I_2 is from 0.2 to 0.8 μm.

79. The semiconductor device according to Claim 76, wherein the difference I_3-I_2 is from 0.2 to 0.8 μm.

80. The semiconductor device according to Claim 77, wherein the difference I_3-I_2 is from 0.2 to 0.8 μm.

81. The semiconductor device according to Claim 75, wherein the difference I_4-I_3 between the spacing I_4 between the third guard ring and the fourth guard ring fourth nearest to the well region and the spacing I_3 between the second guard ring and the third guard ring is 1 μm or less.

82. The semiconductor device according to Claim 76, wherein the difference I_4-I_3 between the spacing I_4 between the third guard ring and the fourth guard ring fourth nearest to the well region and the spacing I_3 between the second guard ring and the third guard ring is 1 μm or less.

83. The semiconductor device according to Claim 77, wherein the difference I_4-I_3 between the spacing I_4 between the third guard ring and the fourth guard ring fourth nearest to the well region and the spacing I_3 between the second guard ring and the third guard ring is 1 μm or less.

84. The semiconductor device according to Claim 81, wherein the difference I_4-I_3 is from 0.2 to 0.8 μm.

85. The semiconductor device according to Claim 82, wherein the difference I_4-I_3 is from 0.2 to 0.8 μm.

86. The semiconductor device according to Claim 83, wherein the difference I_4-I_3 is from 0.2 to 0.8 μm.

87. The semiconductor device according to Claim 34, wherein the number of the guard rings is five or more, and the width of the first guard ring nearest to the well region is wider than the width of the fifth guard ring fifth nearest to the well region.

88. The semiconductor device according to Claim 37, wherein the number of the guard rings is five or more, and the width of the first guard ring nearest to the well region is wider than the width of the fifth guard ring fifth nearest to the well region.

89. The semiconductor device according to Claim 57, wherein the number of the guard rings is five or more, and the width of the first guard ring nearest to the well region is wider than the width of the fifth guard ring fifth nearest to the well region.

90. The semiconductor device according to Claim 87, wherein the number of the guard rings is six or more, and the width of the second guard ring second nearest to the well region is wider than the width of the sixth guard ring sixth nearest to the well region.

91. The semiconductor device according to Claim 88, wherein the number of the guard rings is six or more, and the width of the second guard ring second nearest to the well region is wider than the width of the sixth guard ring sixth nearest to the well region.

92. The semiconductor device according to Claim 89, wherein the number of the guard rings is six or more, and the width of the second guard ring second nearest to the well region is wider than the width of the sixth guard ring sixth nearest to the well region.

93. The semiconductor device according to Claim 90, wherein the number of the guard rings is seven or more, and the width of the third guard ring third nearest to the well region is wider than the width of the seventh guard ring seventh nearest to the well region.

94. The semiconductor device according to Claim 91, wherein the number of the guard rings is seven or more, and the width of the third guard ring third nearest to the well region is wider than the width of the seventh guard ring seventh nearest to the well region.

95 The semiconductor device according to Claim 92, wherein the number of the guard rings is seven or more, and the width of the third guard ring third nearest to the well region is wider than the width of the seventh guard ring seventh nearest to the well region.

96. The semiconductor device according to Claim 34, further comprising an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the well region and the first guard ring nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

97. The semiconductor device according to Claim 37, further comprising an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the well region and the first guard ring nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

98. The semiconductor device according to Claim 57, further comprising an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the well region and the first guard ring nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

99. The semiconductor device according to Claim 96, further comprising an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the first guard ring and the second guard ring second nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

100. The semiconductor device according to Claim 97, further comprising an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the first guard ring and the second guard ring second nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

101. The semiconductor device according to Claim 98, further comprising an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the first guard ring and the second guard ring second nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

102. The semiconductor device according to Claim 99, wherein the number n of the guard rings is three or more and the semiconductor device further comprises an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the second guard ring and the third guard ring third nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

103. The semiconductor device according to Claim 100, wherein the number n of the guard rings is three or more and the semiconductor device further comprises an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the second guard ring and the third guard ring third nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

104. The semiconductor device according to Claim 101, wherein the number n of the guard rings is three or more and the semiconductor device further comprises an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the second guard ring and the third guard ring third nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

105. The semiconductor device according to Claim 102, wherein the number n of the guard rings is four or more and the semiconductor device further comprises an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the third guard ring and the fourth guard ring fourth nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

106. The semiconductor device according to Claim 103, wherein the number n of the guard rings is four or more and the semiconductor device further comprises an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the third guard ring and the fourth guard ring fourth nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

107. The semiconductor device according to Claim 104, wherein the number n of the guard rings is four or more and the semiconductor device further comprises an electrical conductor film above the surface of the breakdown-voltage sustaining layer between the third guard ring and the fourth guard ring fourth nearest to the well region with an insulation film interposed between the electrical conductor film and the surface of the breakdown-voltage sustaining layer.

108. The semiconductor device according to Claim 96, wherein the electrical conductor film is at a floating potential.

109. The semiconductor device according to Claim 97, wherein the electrical conductor film is at a floating potential.

110. The semiconductor device according to Claim 98, wherein the electrical conductor film is at a floating potential.

111. The semiconductor device according to Claim 34, wherein the breakdown-voltage sustaining layer comprises semiconductor regions of the first conductivity type and semiconductor regions of the second conductivity type arranged alternately.

112. The semiconductor device according to Claim 37, wherein the breakdown-voltage sustaining layer comprises semiconductor regions of the first conductivity type and semiconductor regions of the second conductivity type arranged alternately.

113. The semiconductor device according to Claim 57, wherein the breakdown-voltage sustaining layer comprises semiconductor regions of the first conductivity type and semiconductor regions of the second conductivity type arranged alternately.

114. The semiconductor device according to Claim 1, further comprising an organic polymer film protecting the surface of the semiconductor device.

115. The semiconductor device according to Claim 2, further comprising an organic polymer film protecting the surface of the semiconductor device.

116. The semiconductor device according to Claim 34, further comprising an organic polymer film protecting the surface of the semiconductor device.

117. The semiconductor device according to Claim 37, further comprising an organic polymer film protecting the surface of the semiconductor device.

118. The semiconductor device according to Claim 57, further comprising an organic polymer film protecting the surface of the semiconductor device.

Patent Application